INTEGRATED CIRCUIT PACKAGE AND PROCESS FOR FORMING THE SAME

This application claims priority to the provisional patent application entitled, "Package for a Fine Pad Pitch Semiconductor Die and Process for Forming The Same," serial number 60/240,389, filed October 12, 2000.

BRIEF DESCRIPTION OF THE INVENTION

The present invention relates generally to the field of semiconductor packaging. More specifically, the present invention relates to an integrated circuit package and a process for forming the same.

BACKGROUND OF THE INVENTION

Most integrated circuit packages share a substantially standard construction. Specifically, the actual circuitry is on a semiconductor die, which is mounted, usually by adhesive, to a relatively large (as compared to the die) mass or "slug" which acts as a heat sink.

The die has a plurality of bond pads through which power, ground, and signals are communicated outside the die. Bond wires are bonded, typically by a process known as "wirebonding," to the bond pads. The other ends of the bond wires are wirebonded to one of a plurality of metallic lead fingers, or package leads, that lay on

the heat sinking mass but are separated from it by a non-conductive layer. The non-conductive layer is typically an insulating adhesive tape, although it may be other materials such as a ceramic layer bonded to the heat sinking mass.

The package leads are generally formed by stamping from a single sheet of suitable conductive metal. The portions which are to protrude from the package as pins are joined together by a rectangular band of metal at their outer extremities, forming a unit known as a leadframe. To assemble the integrated circuit package, the insulating layer is applied to the heat sinking mass, and the leadframe is attached in place. The die is subsequently affixed, and the wire leads are wirebonded to the appropriate bond pads and package leads.

The entire assembly is then encased in a plastic or epoxy "mold compound" with ends of the package leads protruding as pins for connection to external devices.

As integrated circuit devices become more complex, the die sizes are becoming smaller. Decreasing die sizes have resulted in finer bond pad pitches, longer bond wire lengths, and closer wire-to-wire separation. At the same time, bond wire diameters are becoming thinner.

With the increase of bond wire span, reduction of bond wire diameter, and reduction in wire-to-wire separation, various problems arise in packaging these integrated circuits. One particularly glaring problem is that, when the bond wires are subject to injection molding, adjacent bond wires may come into contact with each other to form short-circuits.

Accordingly, it would be highly desirable to provide an improved integrated circuit package that overcomes the problems associated with increasing bond wire span, reduced bond wire diameter, and reduced wire-to-wire separation.

SUMMARY OF THE DISCLOSURE

The invention provides an improved integrated package and a process for forming the same. According to an embodiment of the invention, a substrate is first provided. A non-conductive lead finger mounting ring is attached to the peripheral region of the substrate. A die attachment pad (DAP) is attached onto the substrate and a plurality of lead fingers are attached to the non-conductive lead finger mounting

ring. A semiconductor die is then attached onto the DAP. Bond wires are attached to the semiconductor die and to the lead fingers. An epoxy material is then dispensed over the semiconductor die, forming a protective encapsulation for the bond wires. The epoxy material is then cured. Thereafter, a mold compound is dispensed and molded to form a plastic encapsulation of the package. The epoxy encapsulation protects the bond wires from the mold compound, and prevents adjacent bond wires from short circuiting during the molding process. Thus, the present invention is particularly applicable to semiconductor dies that have a fine pad pitch.

A completed semiconductor package includes a semiconductor die with bond pads, a die attachment pad on which the semiconductor die is attached, and a substrate on which the die attachment pad is positioned. A non-conductive lead finger mounting ring is attached to the peripheral region of the substrate. Lead fingers are coupled to the lead finger mounting ring, and are coupled to the bond pads via bond wires. The bond wires are enclosed in an epoxy material. The die, the die attachment pad, the substrate, the lead finger mounting ring, and the epoxy material are enclosed in a mold compound.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

Figures 1A-1E are cross-sectional views illustrating steps of an integrated circuit packaging process according to the present invention.

Figures 2A-2B are top views illustrating steps of the integrated circuit packaging process according to the present invention.

Figure 3 is a flow diagram illustrating a process of forming an integrated circuit package according to an embodiment of the invention.

Like reference numerals refer to corresponding parts throughout the drawings.

DETAILED DESCRIPTION OF THE DRAWINGS

Figures 1A-1E are side cross-sectional views illustrating steps of an integrated circuit packaging process in accordance with one embodiment of the present invention. In the following, Figures 1A-1E are discussed in conjunction with Figures 2A and 2B, which are top plan views of Figures 1A and 1C, respectively. Additionally, Figures 1A-1E and 2A-2B are discussed in conjunction with Figure 3, which is a flow diagram depicting the integrated circuit packaging process.

With reference now to Figure 3, the integrated circuit packaging process 300 of the present embodiment begins with providing a substrate having a lead finger mounting ring attached thereto (Box 310). A side view of a substrate 210 having a lead finger mounting ring 220 attached to its periphery is shown in Figure 1A. A top view of the substrate 210 and the lead finger mounting ring 220 is shown in Figure 2A. Although it is shown in Figure 1A and Figure 2A that the lead finger mounting ring 220 is attached to the peripheral region of the substrate 210, it should be understood that the lead finger mounting ring 220 may be attached to other portions of the substrate as well. According to one aspect of the invention, substrate 210 may be conductive or non-conductive, while the lead finger mounting ring 220 is entirely non-conductive, or non-conductive on its top surface 221.

With reference again to Figure 3, the process 300 continues with attaching a Die Attachment Pad (DAP) to the substrate, attaching package leads to the lead finger mounting ring, and attaching a die on the DAP (Box 320). The result of these steps is illustrated in Figure 1B. As shown in Figure 1B, a DAP 230 is attached to a center region of the substrate 210, and package leads 260 are attached to the lead finger mounting ring 220. Furthermore, as shown in Figure 1B, a die 240 is attached to the DAP 230. In an alternate embodiment of the invention, the die 240 is attached directly to the substrate 210 using an insulating epoxy or the like. Additionally, in alternate embodiments, the DAP and the die may be attached to any other region(s) of the substrate.

Referring now to Figure 3 again, the process 300 includes attaching bond wires between bond pads on the die and the package leads (Box 330). This step is sometimes referred to as "wirebonding" and is well known in the art. The result of

this step is illustrated in Figures 1C. As shown in Figure 1C, bond wires 250 are attached between bond pads on the die 240 and the package leads 260. Note that the bond wires 250 are attached to the top surface of the package leads 260 and the top surface of the die 240. Thus, the bond wires 250 are elevated above the lead finger mounting ring 220. A top view of the die assembly of Figure 1C is shown in Figure 2B. Note that, for simplicity, only a few bond pads and a few package leads 260 are illustrated.

With reference yet again to Figure 3, the process 300 includes dispensing sufficient amount of an epoxy material on the die such that the bond wires are encased by the epoxy material (Box 340). The result of this step is illustrated in Figure 1D. As shown in Figure 1D, the top surface of the epoxy material 270 may rise above the die 240 to encase the bond wires 250. The epoxy material 270 may assume an approximately semi-spherical shape. In other words, the epoxy material 270 has an approximately rounded top surface, or a "glob top." Note that the epoxy material 270 is corralled within the area defined by the lead finger mounting ring 220. In this way, run-off of the epoxy material 270 can be prevented. It should also be noted that the shape of the top surface of the epoxy material may be dependent on the surface tension, viscosity, temperature, and other properties of epoxy material and/or assembling environment. Thus, the epoxy material 270 may assume other shapes. For instance, the epoxy material 270 may have a top surface that assumes an approximately semi-elliptical shape. Note that the dispensing step 340 is separate and distinct from an injection molding process step. Specifically, in one embodiment, the epoxy material dispensed during step 340 does not enclose the entire die assembly. Rather, only the die and the bond wires are enclosed.

Epoxy materials are well known in the art, and are commercially available.

Referring again to Figure 3, the process 300 includes curing the epoxy material (Box 350). According to the present embodiment, the epoxy material is cured using well known curing techniques. Thereafter, according to the present invention, a molding process (e.g., an injection molding process) is performed to enclose the die assembly in a mold compound (Box 360). The package leads are separated from the

lead frame and trimmed. The resultant integrated circuit package is illustrated in Figure 1E.

During the molding process, the epoxy material acts as a protective layer that immobilizes the bond wires and prevents them from swaying. The bond wires, immobilized by the epoxy material, are thus prevented from forming short-circuits during the molding process. This aspect of the present invention is especially significant to semiconductor dies having a fine pad pitch (e.g., under 60 μm) and having bond wires that are long (e.g., above 3500 μm) and thin (e.g., wire diameter under 25 μm). It should be noted, however, that the present invention is equally applicable to any other types of semiconductor products.

The present invention, a package for a semiconductor die and process for forming the same, has thus been disclosed. The foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, obviously many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.